REMARKS

Claims 1 and 30 have been amended herein to clarify the particular nature of the ceramic body, which provides a substrate upon which the ceramic coating is disposed. In particular, Claims 1 and 30 have been amended herein to clarify that the ceramic body comprises silicon carbide impregnated with silicon. Description of the silicon impregnation process is provided on page 11, paragraph 36 of the present specification.

1. Claims 1-16, 11-15, 29-30 and 32 were rejected under §103 over Hengst in view of Lu et al. This rejection is respectfully traversed for the following reasons.

Like the present invention, the disclosure of Hengst is drawn to a batch semiconductor processing component, in particular, a wafer boat for supporting a plurality of silicon wafers. As is well understood in the industry, such wafer boats are used in batch processing, typically thermal processing during which a plurality of wafers are simultaneously coated with a CVD coating or an oxidized coating. These batch processes are very well understood in the art and used universally among semiconductor fabs throughout the world. Among the various technical features that are required for such processing, it is generally important to provide wafer boats that can withstand high temperature treatment, and quite importantly, wafer boats that do not contribute to impurity generation during processing. In this latter respect, the industry utilizes wafer boats of materials that have a fairly closely matched thermal expansion coefficient with coatings deposited on the wafers (and the wafer boat) during processing. In this way, residual stresses are minimized in the deposited coating, and flaking or peeling of the coating from the wafer boat is minimized, this flaking or peeling otherwise causing detrimental particle contamination. As should be clear from the foregoing, the particular material requirements of wafer boats used in batch processing are very well defined by the industry.

In the context of batch processing wafer boats, the claimed invention combines several important features, including a ceramic coating having a minimum thickness of 30 microns and surface finish less than or equal to 1.0 micron. Since Hengst fails to disclose or even remotely suggest the claimed combination of features including the recited minimum thickness of 30 microns, the PTO has looked to Lu et al. as a secondary reference. However, Applicant submits that the PTO's reliance upon Lu et al., in an attempt to meet the deficiencies of Hengst, is entirely misplaced.

In contrast to the disclosure of Hengst, as being unequivocally limited to a wafer boat for carrying and processing multiple semiconductor wafers in a batch processing environment, the disclosure of Lu et al. is directed to a single-wafer processing apparatus. While perhaps at first glance the distinction between the batch processing and single-wafer processing components may be overlooked by one not familiar with semiconductor processing, the distinction is very clear and appreciated by those skilled in the art. In the single-wafer processing apparatus of Lu et al., plasma etching is carried out in a process chamber. Plasma etching generally relies on aggressive chemical species such as halogens to remove (rather than deposit) a deposited material, such as SiO_2 or Si_3N_4 deposited in batch processing. In this context, Lu et al. teach that CVD silicon carbide may provide a surface that is resistant to etching, and teaches that the protective silicon carbide coating may have thickness of 100 microns or less, but that many of the embodiments described therein have a thickness of 1 mm or more.

Applicant respectfully submits that one of ordinary skill in the art at the time the invention was made, would not have looked to the disclosure of Lu et al. to set the appropriate thickness for the CVD SiC coating of Hengst. In particular, the CVD SiC coating of Lu et al. is provided for plasma resistance, which is not an issue in batch processing in which semiconductor wafer boats are utilized. As described above, wafer boats are generally used in processes such as deposition. In contrast, the single wafer processing apparatus of Lu et al. utilizes a highly reactive plasma to etch materials during semiconductor patterning operations. One of ordinary skill in the art within the context of semiconductor processing considers the two different disciplines of Hengst and Lu et al. to be entirely distinct, utilizing very different component architectures and different processing environments, and each has unique material demands. Stated alternatively, batch processing that generally employs thermal processing such as deposition is considered to be entirely distinct from plasma processing according to the disclosure of Lu et al.

For at least the foregoing reasons, Applicant submits that one of ordinary skill in the art would not have chosen material thicknesses for a CVD SiC layer of a batch processing wafer boat based upon disclosure of CVD SiC in the context of a single-wafer plasma processing apparatus for etch resistance. The PTO has offered no sound reasoning supported by the references of record as to why one of ordinary skill in the art would have looked to Lu et al. In this regard, the PTO states that thickness employed would be less than 100 microns **"because too thick a layer may have a tendency to peel and too thin layer may not provide adequate protection."** Support for this assertion is nowhere found by the references of record, and support for the asserted reliance upon Lu et al. can only be found from Applicant's own disclosure, which is clearly inappropriate.

Further, the PTO argues that the actual thickness of the CVD SiC layer is an optimization that would be routine for one of ordinary skill in the art. However, Applicant submits that CVD SiC layer thickness has not been recognized by the art of record as being a result-effective variable from which optimization may be carried out. That is, the references of record nowhere even remotely support the PTO's position. Clearly, the references of record draw no significance to the claimed combination of features of minimum thickness and maximum surface finish.

Still further, Applicant submits that Hengst and Lu et al. fail to teach to one of ordinary skill in the art a surface finish of less than 1.0 microns in the context of a ceramic coating. Hengst teaches that arms upon which semiconductor wafers are supported should have a surface roughness (Ra) of no more than 1 micron, while the gist of the disclosure of Hengst is directed to the particular geometric configuration of the wafer boat. In passing, Hengst discloses that the rack material may be CVD coated with refractory material such as silicon carbide. However, the reference does not adequately teach to one of ordinary skill in the art the concept of providing a surface roughness of less than 1 micron in connection with the CVD SiC layer.

In summary, Applicant submits that Hengst and Lu et al. fail to teach or even remotely suggest the claimed combination of surface roughness and thickness features, that one of ordinary skill in the art would not have relied upon the disclosure of Lu et al. for ceramic coating thicknesses, and that the references fail to disclose or suggest surface finish with respect to a ceramic coating. Accordingly, reconsideration and withdrawal of the §103 rejection over Hengst in view of Lu et al. are respectfully requested.

2. Claims 1-6, 9, 11-5, 29-30 and 32 were rejected under 103 over Inaba et al. in view of Lu et al. Applicant respectfully traverses this rejection as well.

Applicant submits that this rejection is deficient for the reasons advanced above with respect to the PTO reliance upon Hengst and Lu et al. In addition, Applicant submits that Inaba et al. fail to disclose or even remotely suggest a feature of the present invention, particularly, a ceramic body comprising silicon carbide impregnated with silicon. Inaba et al. disclose that the substrate may be reaction sintered silicon carbide, referred to as Si-SiC. See column 3, lines 30-33. Although Inaba et al. utilize the term Si-SiC, it is clear that this term is used in connection with reaction sintered silicon carbide. As is well understood in the art, reaction sintered silicon carbide is not the same as or equivalent to silicon impregnated silicon carbide, as claimed. Rather, reaction sintered silicon carbide is formed by a process in which grain growth and densification of a reactive silicon carbide product is formed through heat treatment. No disclosure or suggestion of forming a silicon impregnated silicon carbide body is provided by Inaba et al.

For at least the foregoing reasons and for the reasons discussed above with respect to the Hengst/Lu combination, Applicant respectfully submits that the claimed invention would not have been obvious over Inaba et al. in view of Lu et al. Accordingly, reconsideration and withdrawal of the § 103 rejection over those references is respectfully requested.

3. Claim 16 was rejected under §103 over Inaba et al. in view of Hengst or Wingo. Applicant submits that this rejection is deficient for the reasons advanced above and should be withdrawn as well.

Applicant submits that the present application continues to be in condition for allowance, and accordingly the Examiner is requested to issue a Notice of Allowance for all pending claims. Should the Examiner deem that any further action by the Applicant would be desirable for placing this application in even better condition for issue, the Examiner is requested to telephone Applicant's undersigned attorney at the number listed below.

The Commissioner is hereby authorized to charge any fees, which may be required, or credit any overpayment, to Deposit Account Number 50-2469.

Respectfully submitted,

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